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Data Sheet
April 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

W3030 3 V Dual-Mode IF Cellular Receiver

Features

- Proven double conversion architecture:
  - First IF capability: 10 MHz to over 1000 MHz
  - Second IF capability: 0.2 MHz to 2.0 MHz
- Dual second IF amplifiers and demodulators:
  - Analog-mode limiting amplifier and FM quadrature detector
  - Digital-mode linear AGC amplifiers with dual-mixer I & Q quadrature demodulator
- Accurate, onboard local oscillator phase splitter for digital quadrature demodulator
- Four enable/powerdown modes, selectable from two digital control pins, allow operation with minimal supply current
- Low supply current
- Analog received signal strength indicator (RSSI) available
- Analog AGC for digital-mode IF amplifiers
- Over 100 dB combined voltage gain

Applications

- IS-136 (North American dual-mode) cellular radio portable and mobile terminals
- Cellular radio base stations
- Digital satellite communications
- Multisymbol signaling receivers

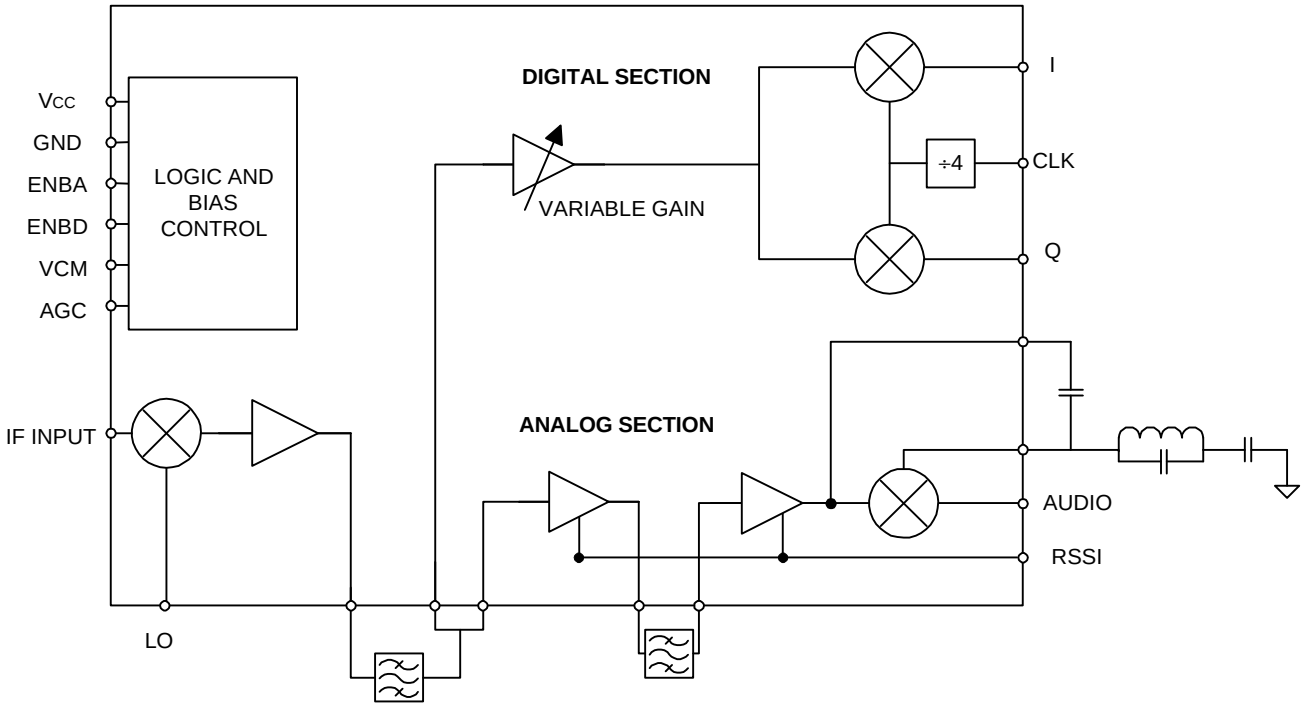

Figure 1. General Block Diagram

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Description

The W3030 is a monolithic integrated circuit that provides most of the receive path functions required to meet the IS-136 (and IS-54) standard. The W3030 converts FM or digitally modulated IF carriers up to 200 MHz and provides required IF gain and separate baseband detectors for the two modulation modes.

The W3030 is organized into three subfunctions (see Figure 2):

1. First IF mixer/amplifier

2. Analog second IF

3. Digital second IF sections

(Note that the electrical specification tables correspond to each subfunction.)

Each section has a buffered output to allow for external filtering, which also provides flexibility in system architecture selection. The first IF mixer section provides 30 dB of fixed voltage conversion gain (power gain = 17 dB). The first IF mixer also performs down-conversion to the 0.2 MHz—2.0 MHz range, which allows the use of inexpensive ceramic filters at two points in the signal path. In the second IF section, the signal path may be split between two parallel amplifier/demodulator sections. In the analog second IF, there is a 40 dB amplifier followed by a 60 dB hard-limiting amplifier and an FM quadrature detector (noncoherent discriminator). The signal path between the 40 dB and 60 dB amplifier stages is brought off-chip for external filtering purposes. In digital mode, an AGC amplifier provides gain between 10 dB and 80 dB. The digital signal is demodulated in double-balanced mixers that are fed with an external local oscillator (LO) signal. The external LO passes through a divide-by-four counter to provide the final IF LO frequency. This architecture greatly reduces the possibility of feedback of the external LO signal to the IF input, which would cause dc offsets at the I & Q outputs. This circuit also provides a 90° phase shift of the LO that is independent of duty cycle. The resulting I & Q differential pairs can be level-shifted using the VCM input pin, providing flexibility in interfacing to digital processing ICs.

A pair of logic inputs allows the device to be put into a powerdown mode and one of two partially enabled modes (analog or digital only), or a fully enabled mode, allowing the use of analog RSSI while in digital receive mode.

Description (continued)

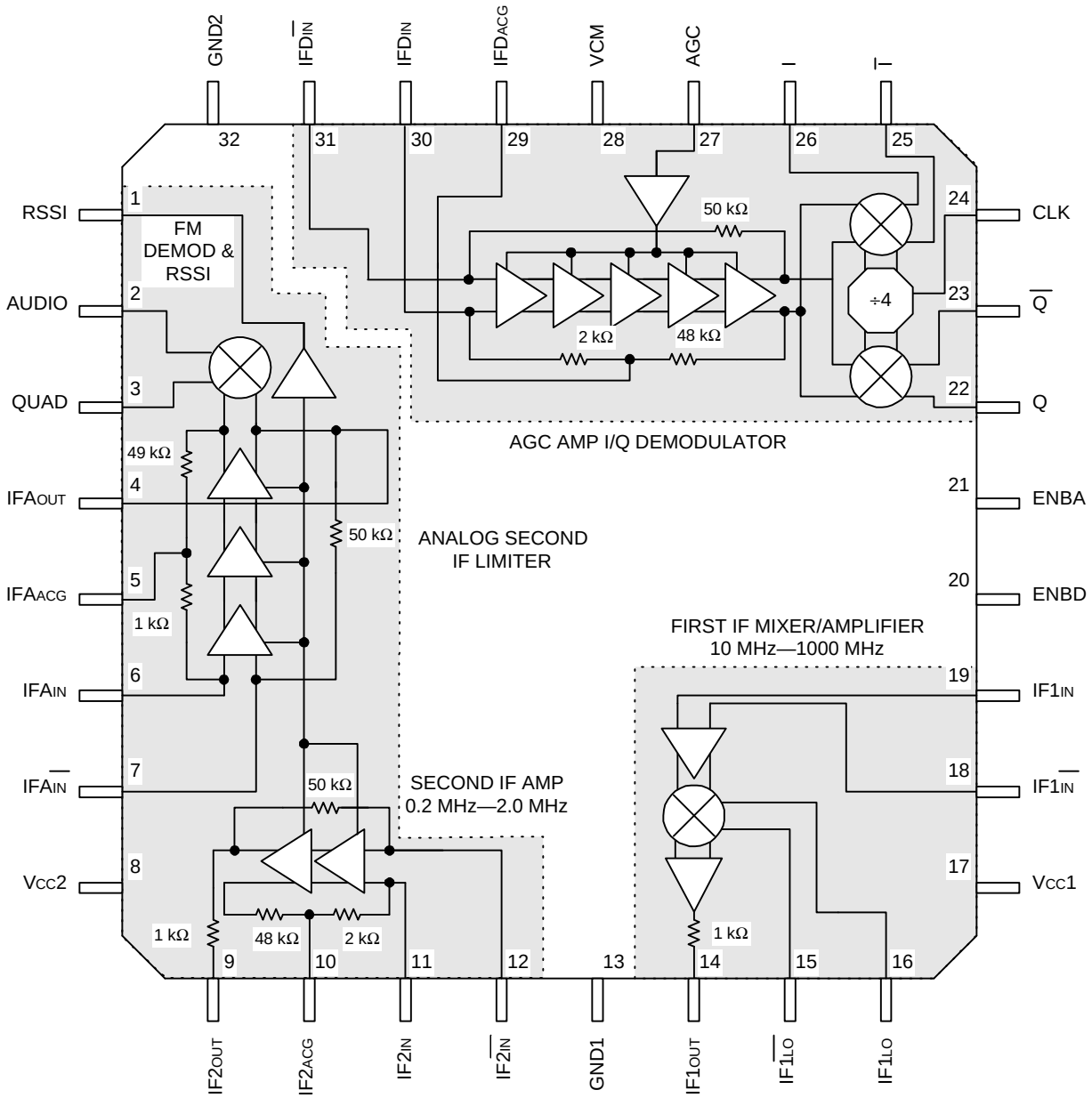


Figure 2. Detailed Block Diagram with Pinout

Pin Information

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Description
1	RSSI	**Received Signal Strength Indicator.** Provides logarithmic (dB-linear) dc output voltage.
2	AUDIO	**Audio Output.** Audio output of FM detector.
3	QUAD	**Quad Input.** Input to FM detector from parallel LC quad coil.
4	IFA_{OUT}	**Analog Output.** Output of analog section limiting amplifiers; couple to quad coil and pin 3 (QUAD) with 10 pF capacitor.
5	IFA_{ACG}	**Analog Signal Ground.** Signal ground for analog section limiting amplifier; connect to ground with 0.1 µF capacitor.
6	IFA_{IN}	**Analog Mode Limiter Input.** Differential input to analog IF limiting amplifier; to be directly coupled to dielectric sources such as ceramic filters. Pin 6 is approximately 1 kΩ with pin 5 ac-grounded.
7	$IFA_{\overline{IN}}$	**Analog Mode Limiter Input (Inverting).** Differential input to analog IF limiting amplifier. To be ac-grounded.
8	$V_{CC}2$	**Second IF Power Supply.** Positive power supply connection for both analog and digital second IF amplifiers and demodulators.
9	$IF2_{OUT}$	**Second IF Output.** Output of 40 dB second IF amplifier; directly couple to dielectric loads such as ceramic filters. Includes internal 1 kΩ termination resistor.
10	$IF2_{ACG}$	**Second IF Signal Ground.** Signal ground for 40 dB second IF amplifier; connect to ground with 0.1 µF capacitor.
11	$IF2_{IN}$	**Second IF Input.** Differential input to 40 dB second IF amplifier; to be directly coupled to dielectric sources such as ceramic filters. Pin 11 is approximately 2 kΩ with pin 10 ac-grounded.
12	$IF2_{\overline{IN}}$	**Second IF Input (Inverting).** Differential input to 40 dB second IF amplifier. To be ac-grounded.
13	GND_1	**First IF Mixer Ground.** Power supply (dc) ground for first IF mixer section.
14	$IF1_{OUT}$	**First IF Mixer Output.** Output of first IF mixer/amplifier section; to be directly coupled to dielectric loads such as ceramic filters. Includes internal 1 kΩ termination resistor.
15	$IF1_{\overline{LO}}$	**First IF Mixer Logical Input (Inverting).** Differential input to first IF mixer local oscillator; to be capacitively coupled to sources with a dc level offset.
16	$IF1_{LO}$	**First IF Mixer Logical Input.** Differential input to first IF mixer local oscillator. To be ac-grounded.
17	$V_{CC}1$	**First IF Mixer Power Supply.** Positive power supply connection for first IF mixer/amplifier section.
18	$IF1_{\overline{IN}}$	**First IF Mixer Input (Inverting).** Differential input to first IF mixer/amplifier section; to be ac-coupled to ground or source.
19	$IF1_{IN}$	**First IF Mixer Input.** Differential input to first IF mixer/amplifier section.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin Number	Pin Name	Pin Description
20	ENBD	**Enable Digital Mode.** Positive logic enable connection for digital mode operation.
21	ENBA	**Enable Analog Mode.** Positive logic enable connection for analog mode operation.
22	Q	**Q Output.** Differential output from Q mixer of quadrature demodulator.
23	$\overline{Q}$	**Q Output (Inverting).** Differential output from Q mixer of quadrature demodulator.
24	CLK	**Clock Input.** Local oscillator (clock) input to quadrature demodulator phase shifter; to be capacitively coupled. Input frequency must be four times second IF center frequency.
25	$\overline{I}$	**I Output (Inverting).** Differential output from I mixer of quadrature demodulator.
26	I	**I Output.** Differential output from I mixer of quadrature demodulator.
27	AGC	**Automatic Gain Control.** AGC control input; to be connected to dc source of 0.25 V—1.55 V.
28	VCM	**Common-Mode Voltage.** Common-mode voltage dc offset set point for I & Q interface, typically $V_{CC}/2$.
29	IFD_{ACG}	**Digital Signal Ground.** Signal ground for digital section limiting amplifier; connect to ground with 0.1 µF capacitor.
30	IFD_{IN}	**Digital Second IF Input.** Differential input to digital section AGC amplifier; to be directly coupled to dielectric sources such as ceramic filters. Pin 30 is approximately 2 kΩ with pin 29 ac-grounded.
31	$IFD_{\overline{IN}}$	**Digital Second IF Input (Inverting).** Differential input to digital section AGC amplifier. To be ac-grounded.
32	GND_2	**Second IF Ground.** Power supply ground for both analog and digital second IF amplifier and demodulator sections.

Table 2. Digital Control Pin Truth Table

Control Pin		Mode/Function
ENBA	ENBD	
LOW	LOW	**All Sleep.** All receive circuits powered down, supply current <10 µA.
LOW	HIGH	**Digital Receive.** First IF mixing stage, AGC amp and I/Q quadrature demodulators active.
HIGH	LOW	**Analog/FM Receive.** First IF mixing stage, 40 dB IF amp, 60 dB limiting amp, RSSI, and FM detector active.
HIGH	HIGH	**All Active.** All receive circuits functional, e.g., digital mode I & Q demodulator used with analog RSSI.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Min	Max	Unit
Ambient Operating Temperature	–35	100	°C
Storage Temperature	–65	150	°C
Lead Temperature (soldering, 10 s)	—	300	°C
Positive Supply Voltage	0	4.5	Vdc
Power Dissipation	—	650	mW
Output Current (continuous)	—	160	mA
ac Peak-to-peak Input Voltage	0	V_{CC}	Vdc
Enable Input Voltage	–0.3	V_{CC} + 0.4	Vdc
VCM, AGC Input Voltage	–0.3	V_{CC} + 0.4	Vdc

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

W3030 ESD Threshold Voltage	
ESD Model	**Rating**
HBM	≥1500 V
CDM	≥1500 V

Operating Ranges

Performance is not guaranteed over the full range of all conditions possible within this table. However, this table lists the ranges of external conditions in which the W3030 provides general functionality, which may be useful in specific applications, without risk of permanent damage. The conditions for guaranteed performance are described below.

Table 3. W3030 Operating Ranges

Parameter	Min	Max	Unit
Supply Voltage	2.7	4.1	Vdc
First IF Mixer/Amplifier Section: Input Frequency Range LO Frequency LO Input Level Range	 10 10 –10	 1000 1000 6	 MHz MHz dBm/50 Ω
Digital Second IF Amplifier, AGC Quadrature Demodulator Section: Second IF Frequency Quadrature Demodulator LO (CLK) Frequency CLK Input Level (square wave)	 0.1 0.4 –10	 4 16 6	 MHz MHz dBm/50 Ω
Analog Second IF Amplifier Frequency	0.1	4	MHz
VCM Input Range	1.25	V_{CC} – 0.8	V

Electrical Specifications

The following apply to all specifications, unless otherwise listed: T_A = 25 °C ± 3 °C; V_{CC} = 2.7 Vdc; $PIF1_{LO}$ = –3 dBm to +3 dBm/50 Ω; IF1 = 10 MHz to 200 MHz; IF2 = 0.2 MHz to 2 MHz; ENBA = ENBD > 1.9 Vdc.

Table 4. dc and Logic Parameters

Parameter	Min	Typ	Max	Unit
Supply Current: Fully Enable (V_{CC} = 3.3) Analog Only Mode (V_{CC} = 3.3) Digital Only Mode (V_{CC} = 3.3) Sleep Mode (V_{CC} = 3.3)	 — — — —	 8 5 5 <1	 11 8 8 10	 mA mA mA µA
V_{IHMIN}	1.9	—	—	V
V_{ILMAX}	—	—	0.7	V
I_{ILMAX} (V_I = 0.7 V)	—	0	10	µA
I_{IHMAX} (V_I = V_{CC})	—	30	250	µA
Enable Time (external capacitor dependent)	—	30	—	µs

Electrical Specifications (continued)

Table 5. First IF Mixer/Amplifier Section

IF deviation = ≤0.5 MHz.

Parameter	Min	Typ	Max	Unit
Voltage Gain (with input matching network from 50 Ω source)	—	30	—	dB
Power Gain	—	17	—	dB
Gain Flatness within IF Deviation	—	±0.2	—	dB
Noise Figure at IF Input (SSB)	—	14	—	dB
1 dB Compression Point at Input to Matching Network	—	–27	—	dBm
IP3 at First IF Matching Network Input	—	–17	—	dBm
IF Input Impedance @ 82 MHz	—	1.7 II 1.8	—	kΩ II pF
LO Input Impedance @ 82 MHz	—	4 II 1.5	—	kΩ II pF
IF Output Impedance	—	1.0	—	kΩ
LO Suppression at IF Input (relative to LO input level)	—	40	—	dB

Table 6. Analog Second IF Amplifier, Limiter, RSSI, FM Detector Section

Filter Z_{IN} = Z_{OUT} = 1.0 kΩ; 6 dB attenuation between 40 dB amplifier output and 60 dB limiting amplifier input; 1 kHz FM at 8 kHz deviation; IF filter bandwidth = 28 kHz. Quad tank Q = 10.

Parameter	Min	Typ	Max	Unit
IF Gain (net) $IF2_{IN}$ to Audio	—	86	—	dB
RSSI Range of Input Signal	65	90	—	dB
RSSI Output Voltage with –20 dBm/50 Ω into $IF1_{IN}$	1.75	2.1	2.6	V
RSSI Output Voltage with –110 dBm/50 Ω into $IF1_{IN}$	0.4	0.7	0.92	V
RSSI Linearity over –100 dBm to –35 dBm into $IF1_{IN}$	—	±0.8	±2.5	dB
RSSI Transfer Function	13	17	25	mV/dB
RSSI Current Capability	—	100	—	µA
IF Input Impedance (40 dB amplifier)	—	2	—	kΩ
IF Output Impedance (40 dB amplifier)	—	1	—	kΩ
IF Input Impedance (60 dB limiter)	—	1	—	kΩ
IF Output Impedance (60 dB limiter)	—	1	—	kΩ
IP3 of 40 dB Amplifier Section (at its output)	—	3	—	dBm
FM Detector Input Impedance (quad, pin 3)	—	40	—	kΩ
Audio Output Impedance	—	500	—	Ω
Audio Output Amplitude ($IF1_{IN}$ = –35 dBm)	150	220	270	mVrms
Audio SINAD for $IF1_{IN}$ = –35 dBm (C-message weighting filter)	32	—	—	dB

Electrical Specifications (continued)

Table 7. Digital Second IF Amplifier, AGC, Quadrature Demodulator Section

P_{CLK} = 320 mVp-p to 640 mVp-p (square wave); IF deviation = ≤0.5 MHz; VCM = 1.3 Vdc to V_{CC} – 0.8 Vdc.

Parameter	Min	Typ	Max	Unit
IF Input Impedance	—	2	—	kΩ
CLK Input Impedance	—	28 II 8.2	—	kΩ II pF
Baseband: –3 dB Bandwidth	—	150	—	kHz
AGC Control Input Resistance	—	500	—	kΩ
AGC Control Voltage Range	—	0.9 ± 0.65	—	Vdc
AGC Transfer Function	11	18	23	mV/dB
AGC Gain Linearity, V_{AGC} = 0.3 to 1.1	—	±1.5	±2.5	dB
I and Q Phase Accuracy	–2	0.4	2	degrees
I and Q ac Amplitude Mismatch	–0.3	±0.05	0.3	dB
I and Q Maximum Output Swing (differential, compressed)	—	2	—	Vp-p
I and Q Common-mode Voltage as Function of VCM, i.e., $\frac{V_I + V_{\bar{I}}}{2}$ or $\frac{V_Q + V_{\bar{Q}}}{2}$	VCM – 0.08	VCM input	VCM + 0.08	Vdc
I and Q Differential Offset Voltage	—	0	35	mV
I and Q Maximum Sink Current per Pin (sum of dc and peak ac)	—	100	—	µA
I and Q Maximum Source Current per Pin (sum of dc and peak ac)	—	1	—	mA
IP3 at Output (I or Q, differential)	—	15	—	dBm/50 Ω
1 dB Compression Point (at output, differential)	—	7	—	dBm/50 Ω
Noise Figure @ IF Input, Differential I + jQ	—	11	—	dB
VCM Input Impedance	—	400	—	kΩ

Table 8. Digital Gain and First IF Mixer Input to Baseband

P_{CLK} = 320 mVp-p to 640 mVp-p (square wave); IF deviation = ≤0.5 MHz; VCM = 1.3 Vdc to V_{CC} – 0.8 Vdc.
Gain numbers include –1.5 dB filter loss.

Parameter	Min	Typ	Max	Unit
Gain V_{AGC} = 1.1 V	91	99	128	dB
Gain V_{AGC} = 0.3 V	36	54	60	dB

RSSI

The RSSI output provides a voltage level that is proportional to the amount of signal present in the analog second IF section. This voltage level is generated internally by summing of the signal current at different points in the 40 dB and 60 dB IF chains. The amount of loss between the 40 dB and 60 dB sections will affect the RSSI linearity. Figure 3 contains two traces of RSSI voltage versus IF input power. One trace is with only the filter loss between the 40 dB and 60 dB amplifiers. The second trace is with a filter and a resistor, to give a total loss of 5.6 dB. The figure indicates a nonlinearity around the –75 dBm input level. This nonlinearity occurs because the 60 dB amplifier chain enters compression, causing less RSSI output. Eventually, as the input signal increases, the 40 dB amplifier will begin to contribute to the total RSSI.

It was determined that 6 dB of interstage loss produces the optimal RSSI response. Most ceramic filters have less than 6 dB insertion loss. Therefore, some additional loss must be inserted in addition to the filter. The simplest way is to use a resistor in series with the filter. This method will cause a mismatch to the filter and may distort its passband response. An L or T configuration may be necessary to provide the required loss without mismatching the filter.

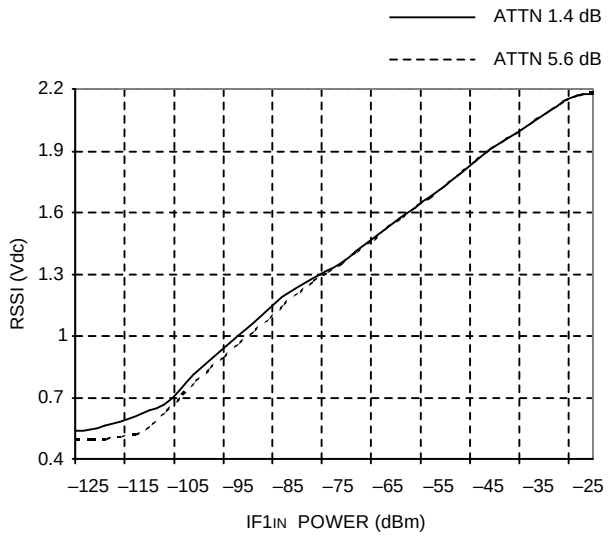


Figure 3. RSSI Out vs. IF1IN Power: 1.4 dB and 5.6 dB Loss Between 40 dB and 60 dB Amplifiers

Quadrature Detector

Figure 4 is a simplified schematic of the quadrature detector of the W3030. The quadrature detector circuit is similar to a mixer; but, instead of mixing two different frequencies, it multiplies two signals of the same frequency that are phase-shifted versions of each other. Multiplying the phase-shifted with the unshifted signals produces the audio portion of the FM signal.

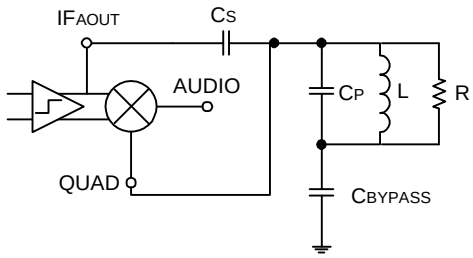


Figure 4. Quadrature Detector

Before the IF signal is differentially applied to the multiplier, the signal is passed through a limiter stage to produce a constant amplitude signal. The same signal is brought out single-ended to pin 4, IFAOUT. The signal at IFAOUT is passed through a phase-shifting network (CS + CP + L + R). The phase-shifted signal is applied back to the lower portion of the multiplier at pin 3, QUAD. The parallel L/C resonant circuit provides frequency selective filtering at the IF frequency. The L/C tank must be ac-grounded at the IF frequency through a dc blocking capacitor (CBYPASS).

Because information in an FM signal is contained in the deviation from the center frequency, the design of the resonant bandpass circuit is very important, particularly the load Q. A higher-loaded Q for a given deviation will produce a larger output signal than a lower Q circuit. However, a high Q circuit will permit only a limited amount of deviation from center frequency before distortion occurs.

Figure 5 illustrates an equivalent quad tank circuit including the W3030 40 kΩ input resistance. Equations 1 and 2 are used to calculate resonant frequency and tank circuit Q.

Quadrature Detector (continued)

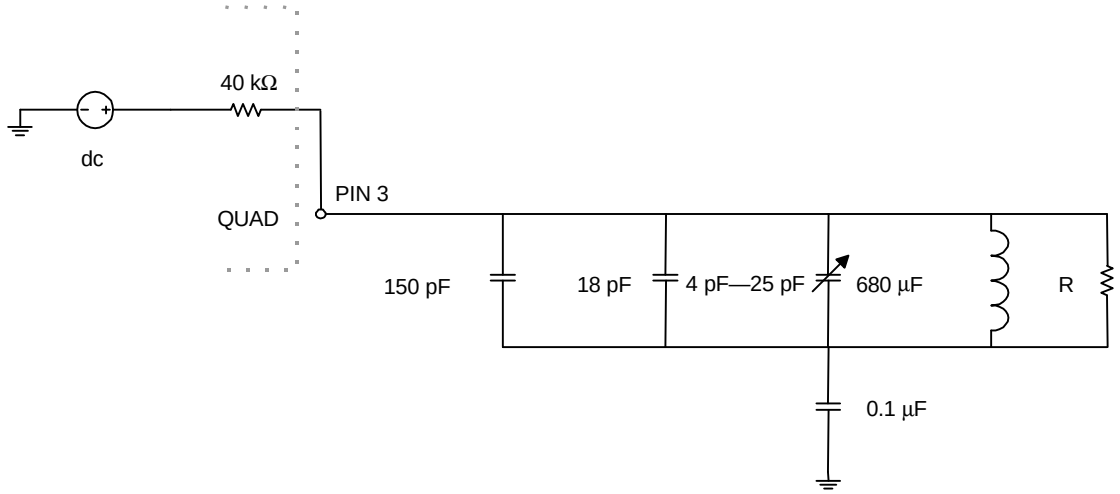


Figure 5. L/C Tank Equivalent Circuit

$$f1 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\left(680 * 6^{-10}\right) * \left(184 * 10^{-12}\right)}} = 450\ \text{kHz} \qquad \text{Equation (1)}$$

$$Q = 2\pi * f * RC = 2\pi * \left(450 * 10^{3}\right) * \frac{\left(40 * 10^{3} * 33 * 10^{3}\right)}{\left(40 * 10^{3} + 33 * 10^{3}\right)} * \left(184 * 10^{-12}\right) = 9.4 \qquad \text{Equation (2)}$$

The W3030 evaluation board is designed with a 450 kHz IF frequency, as shown in our example. The Q of the tank circuit is set to 10 by the external resistor.

Quad Tank S-Curves

One method of determining if the Q of the tank is too large or too small is to produce an S-curve of the quad tank. An S-curve is a plot of the dc audio output voltage versus IF input frequency. With small deviations from center frequency, there is a proportional change in the dc audio output voltage. The overall linearity of the curve is determined by the Q of the tank circuit; therefore, the Q determines how much deviation is allowed before distortion of the audio signal occurs. The L/C tank circuit has a shunt resistor to set the Q of the tank. The procedure to produce these plots is as follows:

1. Remove the 450 kHz IF filter and drive the input of the limiting amplifier with a signal generator capable of FM modulation.
2. Apply FM modulation and adjust the tank capacitor for maximum audio out and minimal distortion.
3. Remove the FM modulation and sweep the IF frequency above and below center frequency while monitoring the dc voltage at the audio output.

The following S-curves were produced with the value of the quad tank resistor varied from 18 kΩ, to 30 kΩ, to removing the resistor. The resistor value of 33 kΩ, which corresponds to a Q of 10, was chosen as the optimal resistor value.

Quadrature Detector (continued)

Quad Tank S-Curves (continued)

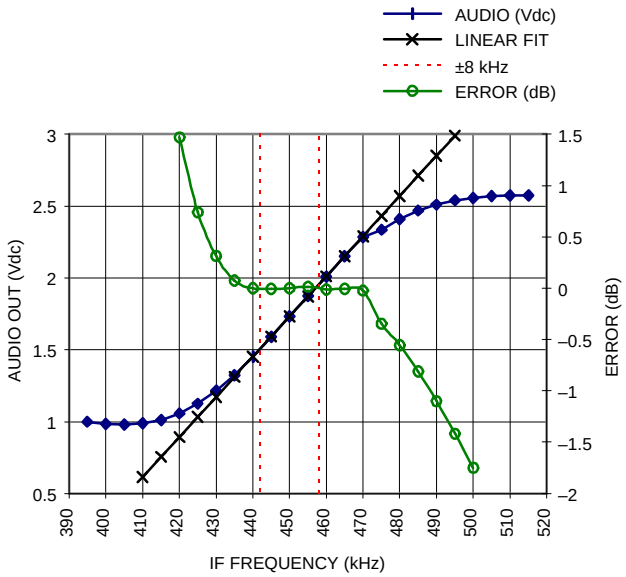


Figure 6. Audio Output vs. IF Frequency, 18 kΩ Quad Tank Resistor

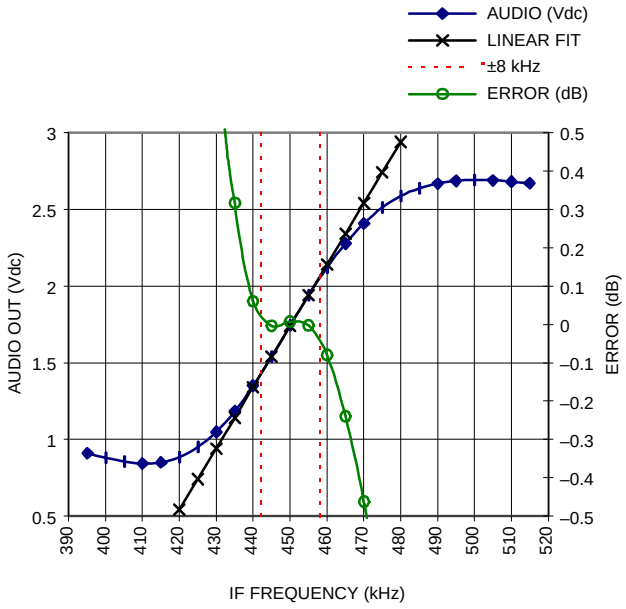


Figure 7. Audio Output vs. IF Frequency, 33 kΩ Quad Tank Resistor

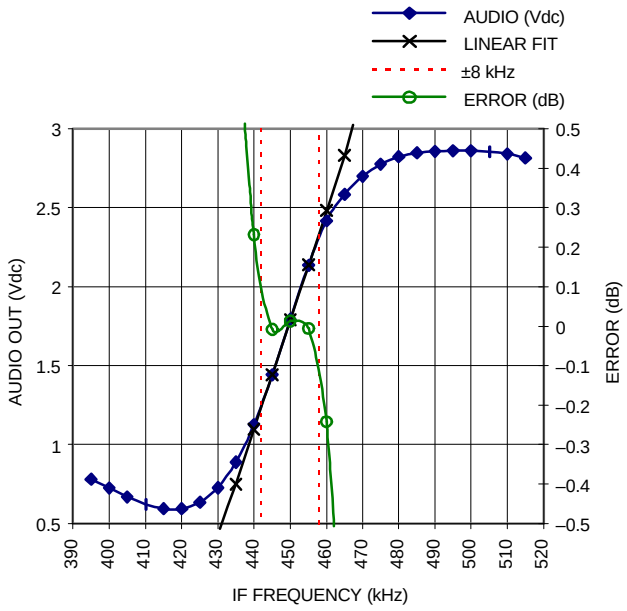


Figure 8. Audio Output vs. IF Frequency, Quad Tank Resistor Removed

Test Circuit Diagram

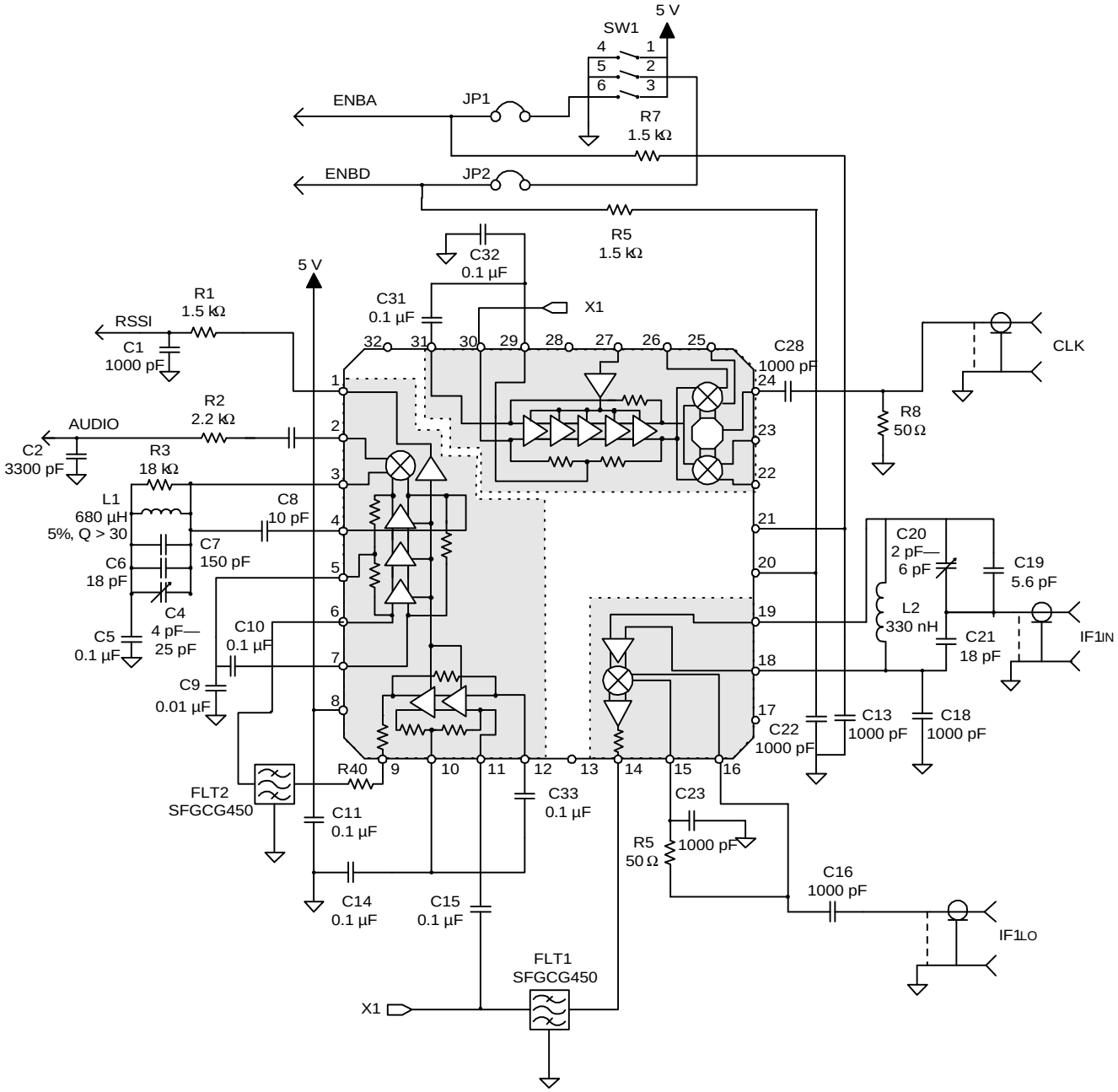


Figure 9. Test Circuit Diagram

Characteristic Curves

Unless otherwise specified, V_{CC} = 2.7 Vdc.

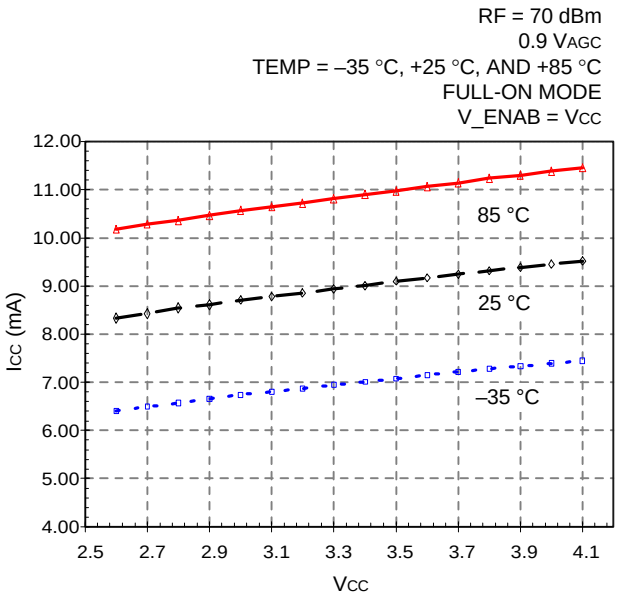


Figure 10. Icc vs. Vcc

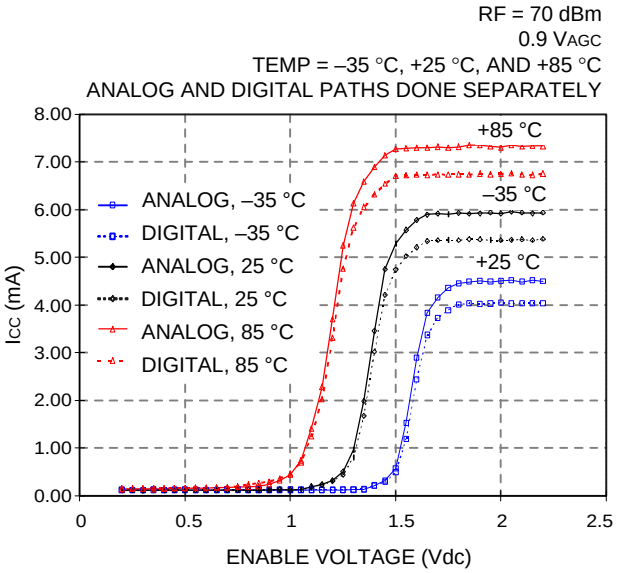


Figure 11. Icc vs. Enable Voltage

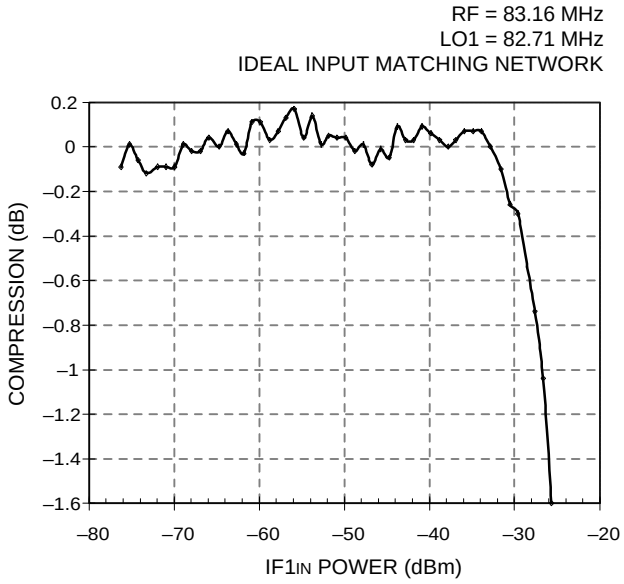


Figure 12. First IF Mixer Output Compression

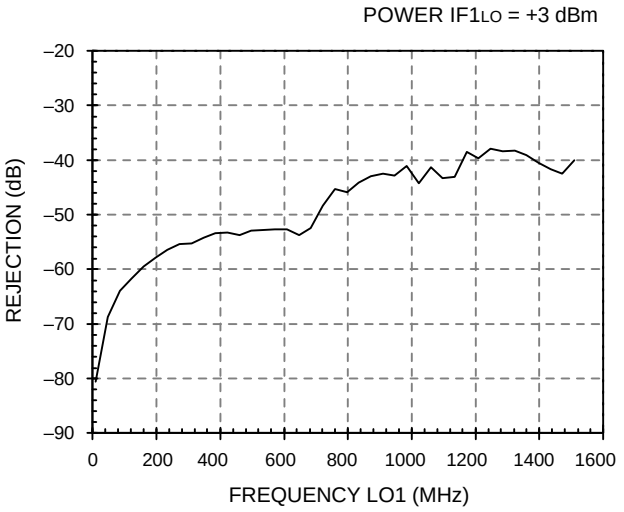


Figure 13. First IF Mixer: LO Rejection at IF Input vs. IF1LO

Characteristic Curves (continued)

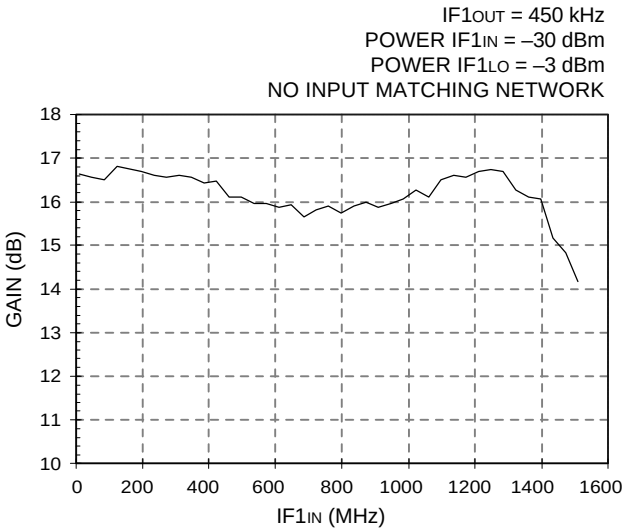


Figure 14. First IF Mixer: Conversion Voltage Gain vs. Frequency IF1IN

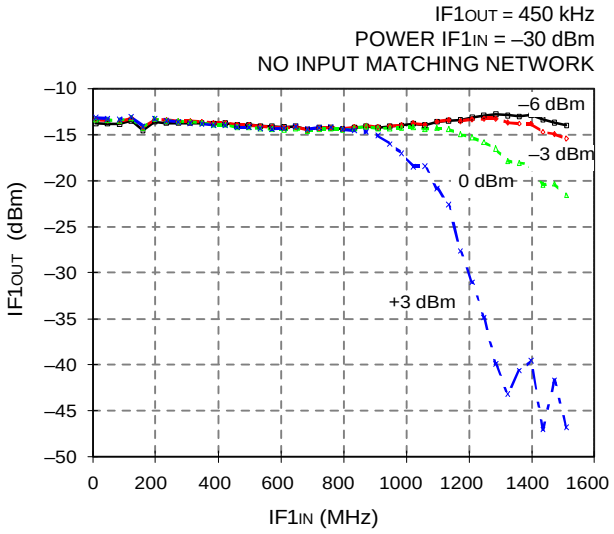


Figure 15. First IF Mixer: IF1OUT vs. IF1IN (LO1 @ –6, –3, 0, +3 dBm)

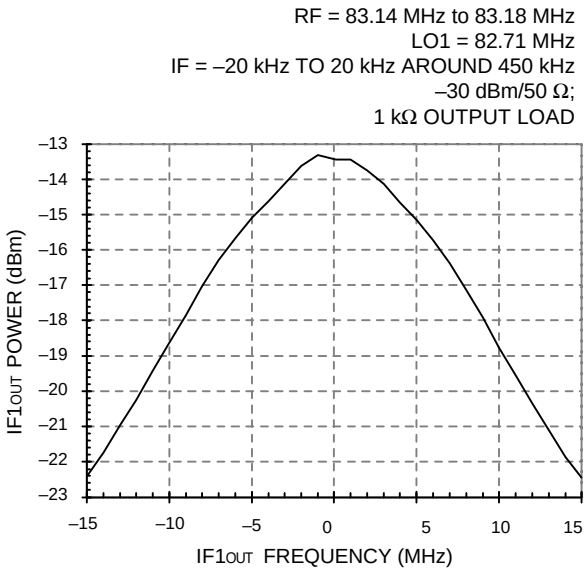

RF = 83.14 MHz to 83.18 MHz
LO1 = 82.71 MHz
IF = –20 kHz TO 20 kHz AROUND 450 kHz
–30 dBm/50 Ω;
1 kΩ OUTPUT LOAD
IF1OUT POWER (dBm)
IF1OUT FREQUENCY (MHz)

Figure 16. First IF Mixer Bandwidth

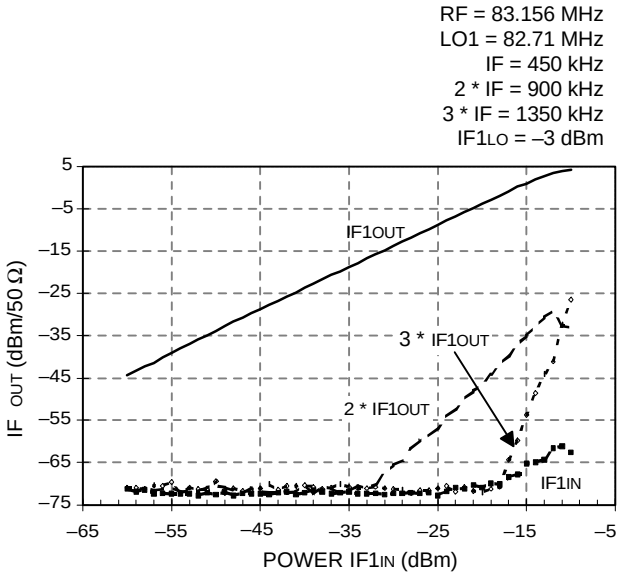


Figure 17. First IF Mixer: Significant Signals vs. Power IF1IN

Characteristic Curves (continued)

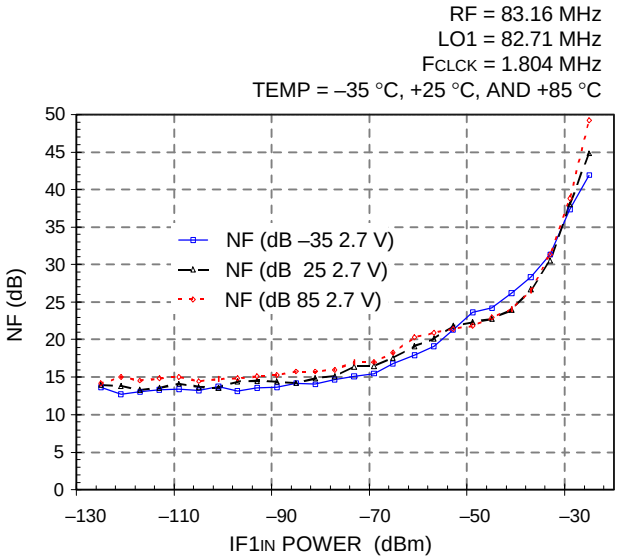


Figure 18. First Mixer and Digital Second IF Section Noise Figure vs. IF1IN Power

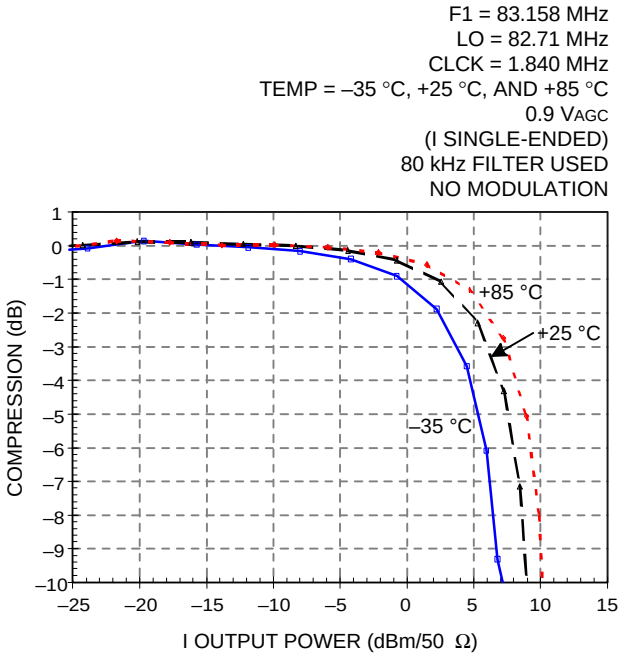


Figure 20. First Mixer and Digital Second IF Section Gain Compression vs. I Output Power

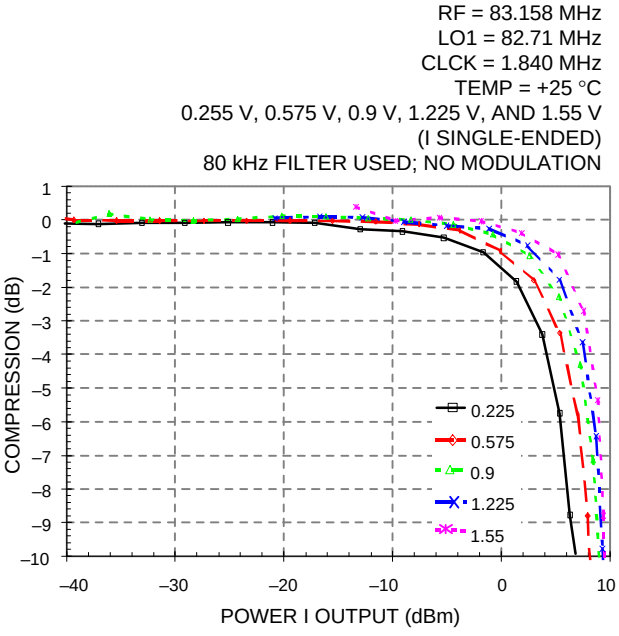


Figure 19. First Mixer and Digital Second IF Section Gain Compression vs. I Output (Single-Ended)

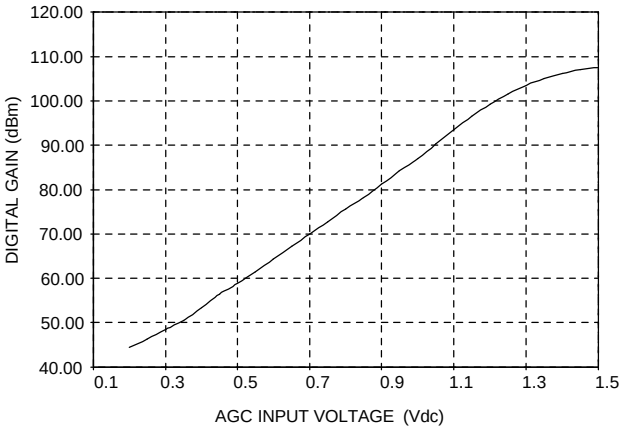


Figure 21. First Mixer and Digital Second IF Section Gain vs. AGC Input (–110 dBm)

Characteristic Curves (continued)

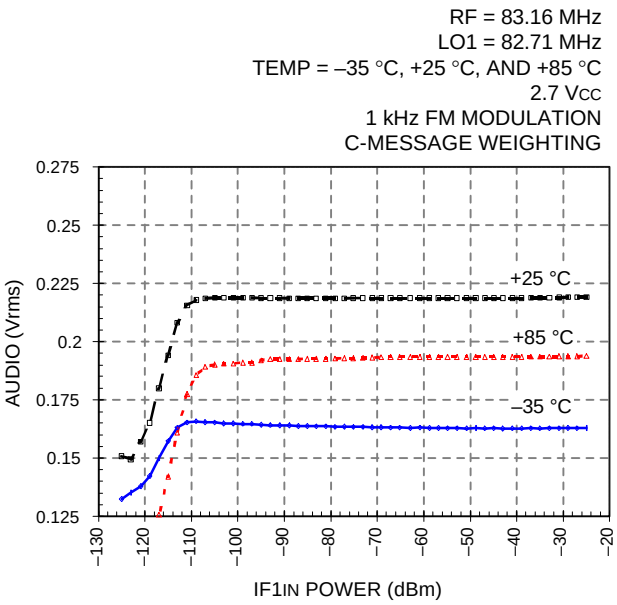


Figure 22. First Mixer and Analog Second IF Section Audio vs. IF1IN Power (2.7 Vcc)

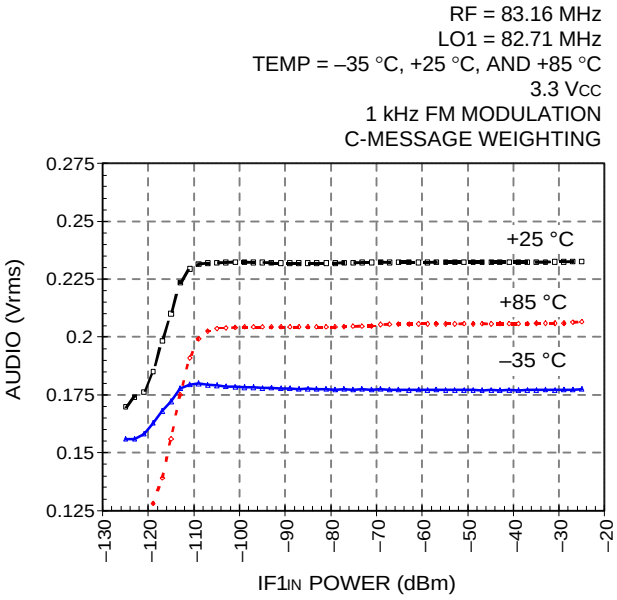


Figure 23. First Mixer and Analog Second IF Section Audio vs. IF1IN Power (3.3 Vcc)

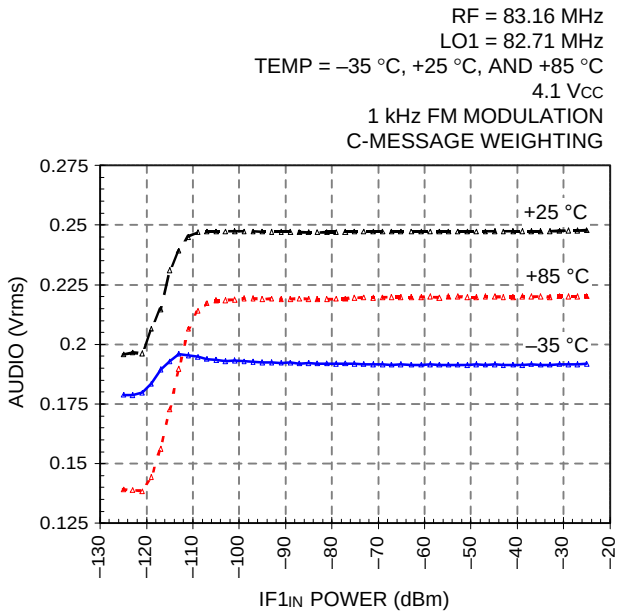
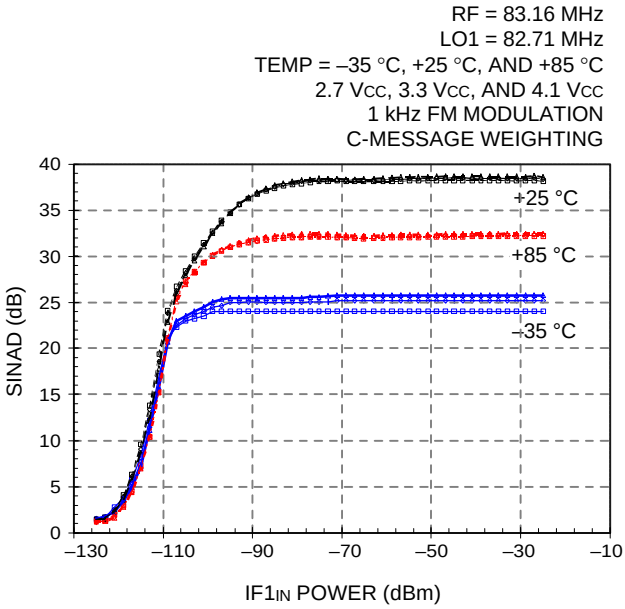


Figure 24. First Mixer and Analog Second IF Section Audio vs. IF1IN Power (4.1 Vcc)



Note: Minimum variation with voltage

Figure 25. First Mixer and Analog Second IF Section SINAD vs. IF1IN Power

Characteristic Curves (continued)

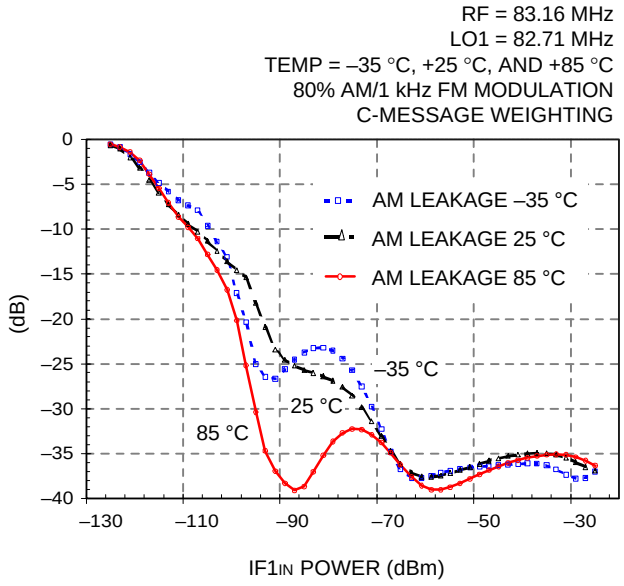


Figure 26. First Mixer and Analog Second IF Section AM Sensitivity (Relative Audio Out) vs. IF1IN Power

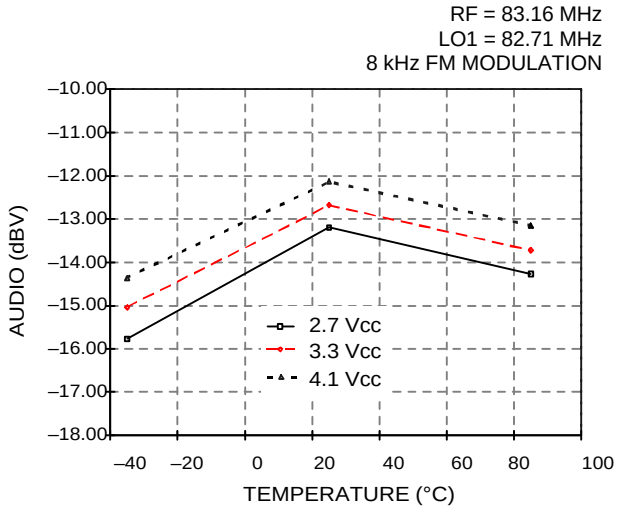


Figure 27. Audio Output vs. Temperature

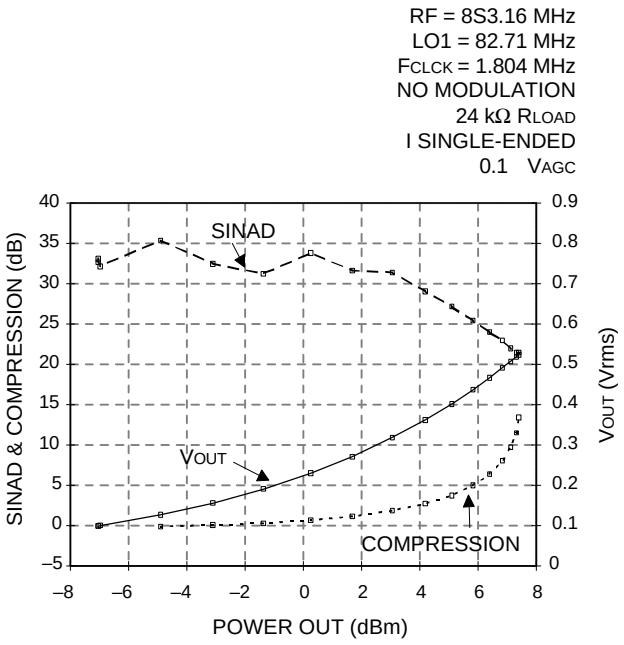


Figure 28. Digital Second IF Section SINAD, Output Voltage, and Compression vs. Output Power

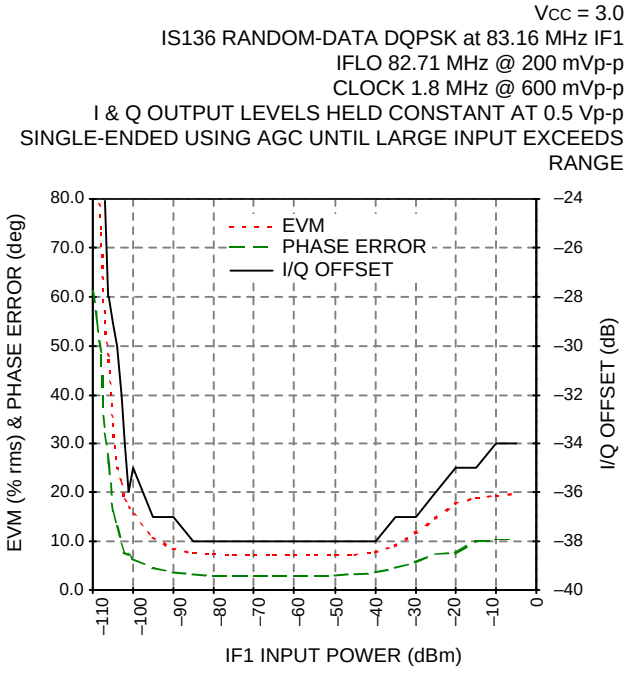
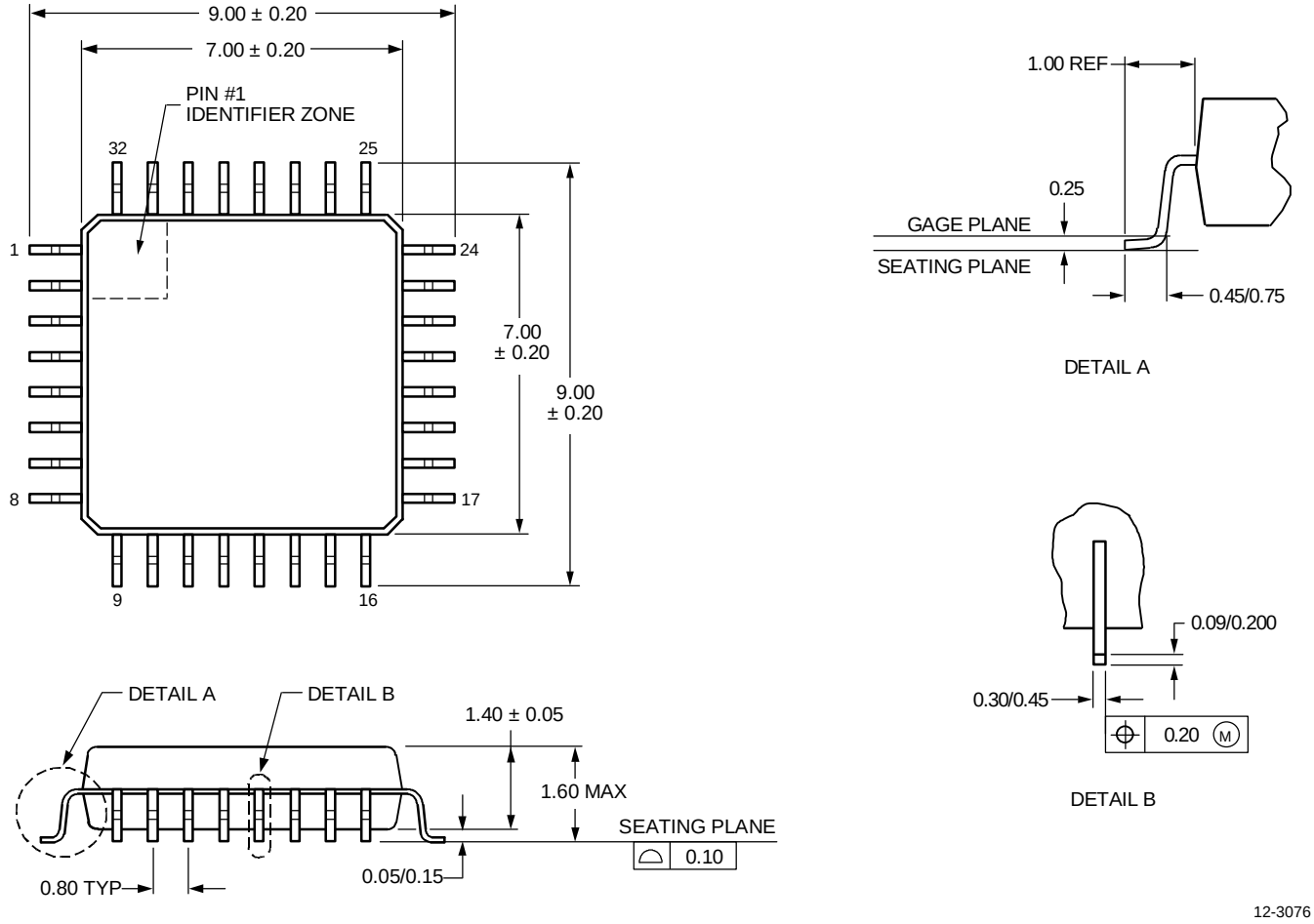

VCC = 3.0
IS136 RANDOM-DATA DQPSK at 83.16 MHz IF1
IFLO 82.71 MHz @ 200 mVp-p
CLOCK 1.8 MHz @ 600 mVp-p
I & Q OUTPUT LEVELS HELD CONSTANT AT 0.5 Vp-p
SINGLE-ENDED USING AGC UNTIL LARGE INPUT EXCEEDS RANGE
EVM
PHASE ERROR
I/Q OFFSET
EVM (% rms) & PHASE ERROR (deg)
I/Q OFFSET (dB)
IF1 INPUT POWER (dBm)

Figure 29. EVM/Phase/Offset vs. IF1 Input Level

Outline Diagram

32-Pin TQFP

Dimensions are in millimeters.



Manufacturing Information

This device will be assembled in one of the following locations: assembly codes P, M, or T.

Ordering Information

Device Code	Description	Package	Comcode
LUCW3030ACA	Bulk Tray	32TQFP	107841082
LUCW3030ACA-DB	Dry Pack	32TQFP	107841090
EVB3030A	Evaluation Board	—	107739377

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April 1999
DS98-399WRF (Replaces DS97-174WRF)

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